insulating layer and the mask layer, the mask layer including an aperture in a region corresponding to an electric connection region of the pad; and

dry etching through the surface of the second insulating layer at the aperture in the mask to form an opening extending through the second insulating layer and the first insulating layer to the pad, wherein an etchant gas comprising CF_4 and O_2 is used to form the opening extending through the second insulation layer, and wherein at least a portion of the opening has a tapered shape.

49. (amended) A method as in claim 48, wherein the dry etching comprises isotropically etching at least a portion of the second insulating layer and anisotropically etching at least a portion of the first insulating layer.

52. (amended) A method as in claim 48, wherein at least a side surface of the second insulating layer surrounding the electric connection region has a tapered surface with an acute angle to the top surface of the pad after the dry etching.

53. (amended) A method as in claim 48, wherein an angle of the side surface of the second insulating layer surrounding the opening is smaller than a tapered angle of a side surface of the first insulating layer surrounding the opening.

54. (amended) A method as in claim 48, wherein an angle between a side surface of the second insulating layer surrounding the opening and a top surface of the pad is in the range of 30° to 60°.

55. (amended) A method as in claim 54, wherein an angle between a side surface of a portion of the first insulation layer surrounding the opening and the top surface of the pad is in the range of 60° to 90°.

56. (amended) A method as in claim 48, wherein a distance between an upper end of a side surface of the first insulating layer surrounding the opening and a lower end of the side surface of the second insulating layer surrounding the opening is in the range of 0 μm to 3 μm.

58. (amended) A method as in claim 48, wherein an aperture formed in the second insulating layer after the dry etching is larger than an aperture formed in the first insulating layer after the dry etching.

61. (amended) A method as in claim 60, wherein the same etchant gas is used to etch the first insulating layer and the second insulating layer.

62. (amended) A method as in claim 61, wherein the first insulating layer and the second insulating layer are etched in a continuous manner.

63. (amended) A method as in claim 48, wherein the first insulating layer and the second insulating layer are etched in a continuous manner.

64. (amended) A method for forming a bonding pad area using a dry etch process, comprising:

forming a conducting pad in electrical contact with an electronic device;

forming a protective insulation layer on a surface of the conducting pad, the protective insulation layer including at least first and second insulating layers, wherein the first insulating layer and the second insulating layer are formed from materials having different compositions, the first insulating layer comprising a silicon oxide layer, the second insulating layer comprising a silicon nitride layer, the silicon oxide layer being formed on the conducting pad, the silicon nitride layer being formed on the silicon oxide layer;

forming a mask in direct contact with a surface of the protective insulation layer and providing an opening in the mask; and

dry etching through the surface of the protective insulation layer at the opening in the

mask to form an aperture extending through the silicon nitride layer and the silicon oxide layer to the surface of the pad using CF_4 and O_2 as an etchant, so that the silicon nitride layer includes a side surface surrounding the aperture, the silicon nitride layer side surface having a tapered shape with an angle in the range of 30 degrees to 60 degrees in relation to the surface of the conducting pad, and the silicon oxide layer includes a side surface surrounding the aperture, the silicon oxide layer side surface having a tapered shape with an angle in the range of 60 degrees to 90 degrees in relation to the surface of the conducting pad.

65. (amended) A method as in claim 64, wherein the protective insulation layer consists of the first insulating layer and the second insulating layer, the first insulating layer consisting of a silicon oxide layer and the second insulating layer consisting of a silicon nitride layer.

66. (amended) A method as in claim 65, wherein the dry etching includes continuously etching the second insulating layer and the first insulating layer.

67. (amended) A method as in claim 64, wherein the dry etching includes isotropic etching of at least part of the silicon nitride layer and anisotropic etching of at least part of the silicon oxide layer.

68. (amended) A method of fabricating a semiconductor device comprising:

forming a pad with a predetermined pattern on an insulating layer;

forming a protective insulating layer on a surface of the pad;

forming a mask layer in direct contact with a surface of the protective insulating layer, the mask layer having an aperture in a region corresponding to an electrical connection region of the pad; and

dry etching through the protective insulating layer using an etchant comprising CF_4 and O_2 to form an opening extending through the protective insulating layer to the electrical connection region of the pad, so that the protective insulating layer includes a side surface

surrounding the opening, the side surface being tapered so that the opening of the protective insulation layer at the pad surface is smaller than the opening of the protective insulation layer a distance away from the pad surface.

70. (amended) The method of fabricating a semiconductor device of claim 68, wherein a tapered angle between the side surface of the insulating layer surrounding the opening is in the range of 10° to 80°.

72. (amended) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer is formed from one of a silicon oxide layer and a silicon nitride layer.

Please add new claims 73-74 as follows:

--73. (new) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer is formed from a silicon oxide layer and a silicon nitride layer, the silicon oxide layer being formed above the pad and the silicon nitride layer formed above the silicon oxide layer.

74. (new) The method of fabricating a semiconductor device of claim 73, wherein the etchant consists of CF_4 and O_2 and the etching is carried out continuously.--

Remarks

Applicant has filed an RCE and this Amendment in response to the Office Action dated October 24, 2001. Claims 50-51 have been canceled without prejudice. Claims 48-49, 52-56, 58, 61-68, 70 and 72 have been amended. New claims 73-74 have been added. Claims 48-49 and 52-74 are currently pending. Reexamination and reconsideration are respectfully requested.

Clam 53 was rejected under 35 U.S.C. 112, second paragraph. Applicant has amended claim 53 to depend from claim 48. Applicant respectfully requests that the rejection be withdrawn.